

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-3 (Canceled).

Claim 4 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second load elements, for giving a given power-supply potential,

wherein said first resistance-adding transistor is an NMOS transistor, and

said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 5 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor is a PMOS transistor, and

said first resistance-adding transistor has its gate electrode directly connected to said power supply.

Claim 6 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising:~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a first power supply connected to said first and second load elements, for giving a given power-supply potential; and

a second power supply connected to said first and second driver transistors, for giving a GND potential,

wherein said first resistance-adding transistor comprises an NMOS transistor having its gate electrode connected to said first power supply, and PMOS transistor having its gate electrode connected to said second power supply.

Claim 7 (Currently Amended): ~~The semiconductor storage device according to claim 3, wherein~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor,

a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor further comprises a channel region having the same conductivity type as said first and second impurity-containing regions, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

Claim 8 (Original): The semiconductor storage device according to claim 7, which comprises a plurality of said first resistance-adding transistors.

Claim 9 (Currently Amended): ~~The semiconductor storage device according to claim 3, wherein~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode

connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node, wherein

said first gate electrode is connected to said second storage node through said first resistance-adding transistor,

said first resistance-adding transistor has a lower absolute value of a threshold voltage than said first and second driver transistors, and

said first resistance-adding transistor has its gate electrode connected to said first or second impurity-containing region.

Claim 10 (Original): The semiconductor storage device according to claim 9, which comprises a plurality of said first resistance-adding transistors.

Claim 11 (Currently Amended): ~~The semiconductor storage device according to claim 3, further comprising~~

A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

a work line connected to gate electrodes of said first and second access transistors,
wherein said first resistance-adding transistor is an NMOS transistor, and
said first resistance-adding transistor has its gate electrode connected to said work
line.

Claim 12 (Currently Amended): The semiconductor storage device according to ~~claim 3~~claim 4, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and
a fourth impurity-containing region connected to said first storage node,
wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 13 (Currently Amended): A semiconductor storage device comprising a static random access memory cell which comprises a first driver transistor, a first load element, and a first access transistor which are connected to each other through a first storage node, and a second driver transistor, a second load element, and a second access transistor which are connected to each other through a second storage node, said first driver transistor having a first gate electrode connected to said second storage node, said second driver transistor having a second gate electrode connected to said first storage node,

said semiconductor storage device further comprising a first resistance-adding transistor having a first impurity-containing region connected to said first gate electrode and a second impurity-containing region connected to said second storage node,

wherein said first gate electrode is connected to said second storage node through said first resistance-adding transistor, said semiconductor storage device further comprising

~~The semiconductor storage device according to claim 3, further comprising:~~

a semiconductor substrate; and

an interlayer insulating film formed on a main surface of said semiconductor substrate,

wherein said first gate electrode is formed on said main surface of said semiconductor substrate with a gate insulating film interposed therebetween,

said second storage node is formed in said main surface of said semiconductor substrate, and

said first resistance-adding transistor is a thin-film transistor formed on said interlayer insulating film.

Claim 14 (New): The semiconductor storage device according to claim 5, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 15 (New): The semiconductor storage device according to claim 6, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 16 (New): The semiconductor storage device according to claim 7, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 17 (New): The semiconductor storage device according to claim 9, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.

Claim 18 (New): The semiconductor storage device according to claim 11, further comprising:

a second resistance-adding transistor having a third impurity-containing region connected to said second gate electrode; and

a fourth impurity-containing region connected to said first storage node,

wherein said second gate electrode is connected to said first storage node through said second resistance-adding transistor.